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Docket No.: 52352-785

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Customer Number: 20277
George Jonathan KLUTH, et al.	:	Confirmation Number: 9267
Serial No.: 10/071,207	:	Group Art Unit: 2822
Filed: February 11, 2002	:	Examiner: GUERRERO, Maria F.

For: METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITH SUPERSATURATED SOURCE/DRAIN EXTENSIONS AND METAL SILICIDE CONTACTS

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith in triplicate is Appellant(s) Appeal Brief in support of the Notice of Appeal filed April 2, 2004. Please charge the Appeal Brief fee of $330.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

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Date: May 10, 2004

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APPEAL BRIEF

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P.O. Box 1450
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Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed April 2, 2004.

I. REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals and interferences.

III. STATUS OF CLAIMS

Claims 1-20 are pending in this application. Claims 19 and 20 are withdrawn from consideration pursuant to a restriction requirement. Claims 1-18 have been finally rejected. It is from the final rejection of claims 1-18 that this appeal is taken.

IV. STATUS OF AMENDMENTS

No amendment has been filed subsequent to the imposition of the final Office Action dated March 19, 2004.

V. SUMMARY OF INVENTION

The present invention addresses and solves problems related to the production of semiconductor devices with improved performance using supersaturated dopant concentration source/drain extensions. A concern with supersaturated dopant concentrations in source/drain extensions is their susceptibility to dopant diffusion when annealed to moderately high temperatures. The present invention provides a method, wherein the source/drain extensions remain in a supersaturated state throughout device processing because lower temperature processing is used after the formation of the supersaturated source/drain extensions (page 5, line 24 to page 6, line 5 of the written description).

An important aim of ongoing research in the semiconductor industry is the reduction in the dimensions of the devices used in integrated circuits. Planar transistors, such as metal oxide semiconductor (MOS) transistors, are particularly suited for use in high-density integrated circuits. As the size of the MOS transistors and other active devices decreases, the dimensions of the source/drain

regions and gate electrodes, and the channel region of each device, decrease correspondingly (page 1, lines 5 to 9 of the written description).

The design of ever-smaller planar transistors with short channel lengths makes it necessary to provide very shallow source/drain junctions. Shallow junctions are necessary to avoid lateral diffusion of implanted dopants into the channel, since such a diffusion disadvantageously contributes to leakage currents and poor breakdown performance. Shallow source/drain junctions have corresponding shallower source/drain extensions. As the depth of the junction decreases, the electrical resistivity of the junction increases. This increase in resistivity is particularly a problem in shallow source/drain extensions. The high resistivity of shallow source/drain regions and extensions is alleviated by supersaturating the dopant concentration in the source/drain regions and extensions (page 1, lines 10 to 19 of the written description).

One of the concerns recognized by the inventors in employing supersaturated source/drain extensions is their susceptibility to deactivation when exposed to moderately high temperatures, such as those typically employed in cobalt silicide or titanium silicide processing. High temperature annealing during the silicide formation step increases lateral and vertical diffusion of the dopants in the source/drain regions and extensions. Increased vertical diffusion of the dopant results in slower, deeper junctions, while increased lateral diffusion of the dopant can result in junction leakage. Furthermore, every time a wafer is heated and cooled crystal damage from dislocations occur. A high concentration of dislocations can cause device failure from leakage currents (page 3, lines 3 to 10 of the written description).

Supersaturated source/drain extensions can be maintained throughout subsequent processing steps by the present invention, which provides a method of manufacturing a semiconductor device comprising providing a silicon-containing substrate having an upper surface. The silicon containing

substrate comprises a gate electrode formed on the upper surface of the substrate with a gate insulating layer therebetween. The gate electrode has an upper surface and opposing side surfaces. Source/drain regions are in the substrate spaced apart from the gate electrode. Supersaturated dopant concentration source/drain extensions are formed in the substrate between the source/drain regions and the gate electrode. Metal silicide contacts are formed on the upper surfaces of the gate electrode and the substrate in a manner sufficient to maintain the supersaturated dopant concentration in the source/drain extensions (page 3, line 33 to page 4, line 7 of the written description).

The earlier stated needs are further met by another embodiment of the present invention that provides a method of manufacturing a semiconductor device comprising providing a silicon-containing semiconductor substrate and forming a gate oxide layer on the semiconductor substrate. A conductive gate material layer is formed over the gate oxide layer. The gate material layer and gate oxide layer are patterned to form a gate electrode having an upper surface and opposing side surfaces, with a gate oxide layer thereunder. A layer of insulating material is deposited over the gate electrode and semiconductor substrate. The insulating material is patterned to form sidewall spacers on the opposing side surfaces of the gate electrode. Source/drain regions are formed by ion implanting a dopant into the substrate. The sidewall spacers are removed and the substrate is heated to activate the source/drain regions. A supersaturated dopant concentration source/drain extensions are formed between the gate electrode and source/drain regions. A second layer of insulating material is deposited over the gate electrode and semiconductor substrate. The second layer of insulating material is patterned to form sidewall spacers on the opposing side surfaces of the gate electrode. A metal layer is deposited over the gate electrode upper surface, sidewall spacers, and substrate upper surface. The metal layer is heated at a temperature to react with underlying silicon to form metal silicide contacts on the gate electrode and substrate upper surfaces without reducing the dopant concentration in the source/drain

extensions below a supersaturated dopant concentration. The metal that did not react to form metal silicide is removed (page 4, lines 16 to 33 of the written description).

This invention addresses the need of preventing dopant diffusion and deactivation of supersaturated source/drain extensions.

VI. ISSUES

A. The Rejections

Claims 1-3 and 5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Bai (U.S. Patent No. 5,889,331) in view of Applicant admitted prior art (AAPA).

Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Bai in view of AAPA and further in view of Hsu (U.S. Patent No. 5,491,099).

Claims 6 and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Bai in view of AAPA and further in view of Murthy et al. (U.S. Patent No. 6,235,568).

Claims 8 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Bai in view of AAPA and further in view of Tsukamoto (U.S. Patent No. 5,399,506).

Claims 10 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Bai in view of AAPA and further in view of Ozturk et al. (U.S. Patent No. 5,242,847).

Claims 12 and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Bai in view of AAPA and Hsu.

Claims 14 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Bai, AAPA, and Hsu and further in view of Ozturk et al.

Claims 16 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Bai,

AAPA, and Hsu and further in view of Tsukamoto.

Claim 18 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Bai, AAPA, and Hsu and further in view of Murthy et al.

B. The Issues

The Issues that arise in this appeal that require resolution by the Honorable Board of Appeals and Interferences (the Board) are:

Whether claims 1-3 and 5 are unpatentable under 35 U.S.C. § 103(a) for obviousness as predicated upon the combination of Bai and AAPA.

Whether claims 4, 12, and 13 are unpatentable under 35 U.S.C. § 103(a) for obviousness as predicated upon the combination of Bai, AAPA, and Hsu.

Whether claims 6 and 7 are unpatentable under 35 U.S.C. § 103(a) for obviousness as predicated upon the combination of Bai, AAPA, and Murthy et al.

Whether claims 8 and 9 are unpatentable under 35 U.S.C. § 103(a) for obviousness as predicated upon the combination of Bai, AAPA, and Tsukamoto.

Whether claims 10 and 11 are unpatentable under 35 U.S.C. § 103(a) for obviousness as predicated upon the combination of Bai, AAPA, and Ozturk et al.

Whether claims 14 and 15 are unpatentable under 35 U.S.C. § 103(a) for obviousness as predicated upon the combination of Bai, AAPA, Hsu, and Ozturk et al.

Whether claims 16 and 17 are unpatentable under 35 U.S.C. § 103(a) for obviousness as predicated upon the combination of Bai, AAPA, Hsu, and Tsukamoto.

Whether claim 18 is unpatentable under 35 U.S.C. § 103(a) for obviousness as predicated upon the combination of Bai, AAPA, Hsu, and Murthy et al.

VII. GROUPING OF CLAIMS

There are four groups of claims as described below:

Group I - Claims 1-3, 5, 10, 11, 14, and 15;

Group II - Claims 4, 12, and 13;

Group III - Claims 6, 7, and 18; and

Group IV - Claims 8, 9, 16, and 17.

All the claims within a group stand or fall together. Each individual group stands or falls separately from each other group. Separate arguments in support of each group are presented *infra.*

VIII. THE ARGUMENT

A. The Examiner's Position

As regards claims 1-3 and 5, the Examiner asserted that Bai teaches a semiconductor substrate with a gate electrode, source/drain regions, and nickel silicide contact regions formed in a manner sufficient to maintain the dopant concentration in the source/drain extensions. The Examiner acknowledged that Bai does not disclose the required supersaturated dopant concentration. However, the Examiner asserted that admitted prior art teaches forming supersaturated dopant concentration on the extension to reduce the resistivity of the extensions. Therefore, the Examiner concludes it would have been obvious to recognize that the dopant concentration taught by Bai is supersaturated to provide a method of forming reduced resistivity extensions while maintaining the thickness of the silicide layer.

As regards claims 4 , 12, and 13, the Examiner acknowledged that Bai and the alleged AAPA do not disclose removing the spacers prior to forming the source/drain extensions. The Examiner relied on Hsu as supposedly providing a teaching of removing spacers prior to forming source/drain extensions and subsequently forming second sidewall spacers. The Examiner concluded that it would have been obvious to combine the teachings of Hsu with Bai and the alleged AAPA to obtain the claimed method in order to reduce the risk of hot electron reliability failures.

As regards claims 6 and 7, the Examiner acknowledged that the combination of Bai and the alleged AAPA does not disclose the time and concentration as claimed. The Examiner relied on Murthy et al. to conclude that the time and concentration would have been obvious. The Examiner asserted that one of ordinary skill in this art would have combined the Murthy et al. teaching in order to obtain a high dopant concentration as taught by Bai.

As regards claims 8 and 9, the Examiner acknowledged that Bai and the alleged AAPA do not disclose employing laser radiation with the specific energy as claimed. The Examiner relied on Tsukamoto to provide a teaching of pulsed laser irradiation of source/drain regions. The Examiner concluded that it would have been obvious to combine the teachings of Tsukamoto with Bai and the alleged AAPA to obtain the claimed method in order to reduce leakage current.

As regards claims 10 and 11, the Examiner acknowledged that Bai and the alleged AAPA does not disclose forming the source/drain extensions by doped selective epitaxy, as claimed. The Examiner relied on Ozturk et al. to provide a teaching of doped selective epitaxy. The Examiner concluded that it would have been obvious to combine the teachings of Ozturk et al. with Bai and the alleged AAPA to obtain the claimed method in order to form doped shallow regions.

As regards claims 14 and 15, the Examiner acknowledged that the combination of Bai, the alleged AAPA, and Hsu does not disclose forming the source/drain extensions by doped selective

epitaxy, as claimed. The Examiner relied on Ozturk et al. to provide a teaching of doped selective epitaxy. The Examiner concluded that it would have been obvious to combine the teachings of Ozturk et al. with Bai and the alleged AAPA to obtain the claimed method in order to form doped shallow regions.

As regards claims 16 and 17, the Examiner acknowledged that the combination of Bai, the alleged AAPA, and Hsu does not disclose employing laser radiation with the specific energy as claimed. The Examiner relied on Tsukamoto to provide a teaching of pulsed laser irradiation of source/drain regions. The Examiner concluded that it would have been obvious to combine the teachings of Tsukamoto with Murthy et al. to obtain the claimed method in order to reduce leakage current.

As regards claim 18, the Examiner acknowledged that the combination of Bai, the alleged AAPA, and Hsu does not disclose the concentration as claimed. The Examiner relied on Murthy et al. to conclude that the concentration would have been obvious. The Examiner asserted that one of ordinary skill in this art would have combined the Murthy et al. teaching in order to obtain a high dopant concentration as taught by Bai.

B. Appellants' Position

These rejections should be reversed by the Honorable Board because the Examiner has not presented a *prima facie* case of obviousness. The Examiner has not shown that the use of supersaturated source/drain extensions to reduce resistivity of the extensions is prior art. Contrary to the Examiner's assertion, Appellants have not admitted that forming supersaturated dopant concentration in source/drain extensions to reduce resistivity of the extensions is prior art.

The Examiner deemed Appellants' disclosure on page 1 of the instant specification as admitted prior art. However, there is no admission by Appellants in the instant specification that forming supersaturated dopant concentration in source/drain extensions to reduce resistivity of the extensions is prior art. The Examiner is improperly using Appellants' specification against Appellants. 35 U.S.C. § 103(a) statutorily requires that rejections be based on prior art. The Examiner has not based the instant rejections on prior art, as Appellants have not admitted that forming supersaturated dopant concentration in source/drain extensions to reduce resistivity of the extensions is prior art. This rejection is clearly untenable and should be withdrawn.

The Examiner has incorrectly applied the reasoning in *In re Nomiya*, 509 F.2d 566, 184 USPQ 607 (C.C.P.A. 1975) against Appellants. The Examiner's Response to Arguments in the final rejection illustrates why the Examiner's conclusion is incorrect. The Examiner, citing to *Nomiya*, states "[w]hen applicant states that something is prior art, it is taken as being available as prior art against the claims." Appellants, however, have not stated that forming supersaturated source/drain extensions to reduce resistivity of the source/drain extensions is admitted prior art.

The Examiner asserted that because Appellants' disclosure on page 1 of the instant specification was not described as "applicant work" it is admitted prior art. The Examiner has not provided any authority that supports the Examiner's premise that portions of the specification not described as "applicant work" is admitted prior art. The reasoning in *In re Nomiya* is not applicable because *Nomiya* dealt with the situation where the applicant expressly labeled figures in the application "prior art." Appellants have not made any admission, express or implied, that forming supersaturated source/drain extensions to reduce resistivity of the source/drain extensions is prior art.

The Examiner has improperly placed on Appellants the burden of proving that a disclosure in the specification is not prior art. The Examiner, however, has the burden of first showing that

Appellants' have made an admission of prior art. The Examiner has not carried the burden of establishing an admission of prior art, therefore the Examiner has not made a *prima facie* case of obviousness of the claimed methods.

The present invention is further distinguishable over the cited prior art because Bai and the Examiner alleged AAPA, whether taken alone, or in combination do not suggest the claimed method. The Examiner asserted motivation for combining Bai with the alleged AAPA is unrelated to supersaturated source/drain extensions. The Examiner asserted motivation is found in Bai. Bai teaches a processes of forming salicides wherein the thickness of the silicide layer of the conductive layer is greater than the thickness of the silicide layer in the diffusion region of a device. Bai is unconcerned with supersaturated source/drain extensions. Neither the silicide layer over the conductive layer nor the silicide layer over the diffusion regions of Bai overlies the extensions. It is not seen how the asserted motivation in Bai would suggest to one of skill in this art to form supersaturated source/drain extensions.

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge readily available to one of ordinary skill in the art. *In re Kotzab*, 217 F.3d 1365, 1370 55 USPQ2d 1313, 1317 (Fed. Cir. 2000); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). There is no suggestion in Bai or the alleged AAPA to modify the process of Bai to form supersaturated source/drain extensions, as required by claim 1. The mere fact that references can be combined or modified does not render the resulting combination obvious unless the prior art also suggests the desirability of the modification. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

The requisite motivation to support the ultimate legal conclusion of obviousness under 35 U.S.C. § 103 is not an abstract concept, but must stem from the applied prior art as a whole and realistically impel one having ordinary skill in the art to modify a specific reference in a specific manner to arrive at a specifically claimed invention. *In re Deuel*, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995); *In re Newell*, 891 F.2d 899, 13 USPQ2d 1248 (Fed. Cir. 1989). Accordingly, the Examiner is charged with the initial burden of identifying a source in the applied prior art for the requisite realistic motivation. *Smiths Industries Medical System v. Vital Signs, Inc.*, 183 F.3d 1347, 51 USPQ2d 1415 (Fed. Cir. 1999); *In re Mayne*, 104 F.3d 1339, 41 USPQ2d 1449 (Fed. Cir. 1997). There is no motivation for modifying the Bai process to form supersaturated source/drain extensions, as required by claim 1.

The only teaching of the claimed method wherein supersaturated dopant concentration source/drain extensions are formed and metal silicide contacts are formed in a manner sufficient to maintain the supersaturated dopant concentration is found in Appellants' disclosure. However, the teaching or suggestion to make a claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on appellants' disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). As the Examiner acknowledged basing the rejection on Appellants' disclosure, it is clear that the Examiner has relied on impermissible hindsight reasoning.

Claims 4, 12, and 13 are allowable for at least the same reasons as discussed *supra* regarding claim 1. The combination of Hsu and Bai and the alleged AAPA does not suggest the claimed method of manufacturing a semiconductor device. Hsu does not cure the deficiencies of Bai and the alleged AAPA. Hsu does not suggest forming supersaturated dopant concentration source/drain extensions in the substrate between the source/drain regions and the gate electrode, and forming metal silicide contacts on the gate electrode and the substrate in a manner sufficient to maintain the supersaturated

dopant concentration in the source/drain extensions, as required by independent claims 1 and 12. Hsu teaches away from forming supersaturated source/drain extensions, as Hsu expressly teaches forming lightly doped drains (LDD) that are subsequently exposed to high temperature (column 4, lines 3-14).

A prior art reference must be considered in its entirety, i.e., as a **whole**, including portions that would lead away from the claimed invention. Such a teaching away from a claimed invention constitutes potent evidence of non-obviousness. See, for example, *In re Bell*, 991 F.2d 781, 26 USPQ2d 1529 (Fed. Cir. 1993); *In re Hedges*, 783 F.2d 1038, 228 USPQ 685 (Fed. Cir. 1986); *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). Hsu teaches forming LDD regions that are subsequently exposed to high temperature. Hence, Hsu teaches away from the claimed method, and it would not be obvious to combine Hsu with Bai to achieve the claimed method.

In addition, claims 4, 12, and 13 are separately patentable because Hsu discloses first forming the silicide contacts and then subsequently removing the first sidewall spacers (column 3, line 46 to column 4, line 2), whereas claims 4, 12, and 13 require that the silicide contacts are formed **after** the first sidewall spacers are removed.

Claims 6, 7, and 18 are allowable because Murthy et al. do not cure the deficiencies of Bai. In addition, claims 6, 7, and 18 are separately patentable because Murthy et al. teach implanting dopant in the range of approximately $1x10^{20}$-$2.5x10^{21}/cm^3$ in the N-tip regions 212 and in the range of approximately $1x10^{20}$-$5x10^{21}/cm^3$ in the P-tip regions 216 (column 5, lines 3-16 and lines 33-38). Murthy et al., however, teach that the dopant in the N-tip and P-tip regions is diffused out from the implant region when the implants are subsequently annealed (column 5, lines 16-18 and lines 37-40; and column 6, lines 46-53). Thus, Murthy et al. do not maintain supersaturated dopant concentration in the source/drain extensions, as required by independent claims 1 and 12, or the concentration of dopant

required by claims 6, 7, and 18.

The section of Murthy et al. cited by the Examiner as teaching the claimed dopant concentration in the source/drain extensions (column 6, lines 20-30), actually teaches the implanted dopant concentration in the source/drain regions, not the extensions. Further, as explained *supra,* Murthy et al. teach that the dopant is subsequently diffused out from the implant region in an annealing step (column 6, lines 27-29 and lines 46-53). In addition, Murthy et al. teach additional high temperature processing steps of the semiconductor device before the silicide contacts are formed. For example, Murthy et al. disclose forming spacer layer 218 at a temperature of approximately 800 °C (column 5, line 60 to column 6, line3). Rather than teaching that the dopant concentration is maintained in the source/drain extensions, Murthy et al. **explicitly teach diffusing the dopant** out from the source/drain regions and source/drain extensions. It is clear that the source/drain extensions in the Murthy et al. device are not supersaturated when the silicide contacts are formed.

Claims 8, 9, 16, and 17 are allowable because Tsukamoto does not cure the deficiencies of Bai. Tsukamoto does not suggest forming supersaturated dopant concentration source/drain extensions in the substrate between the source/drain regions and the gate electrode, as required by independent claims 1 and 12. Tsukamoto teaches away from forming supersaturated source/drain extensions, as Tsukamoto expressly teaches forming Lightly Doped Drain-source (LDD) that undergo high temperature annealing (column 4, lines 3-11).

A prior art reference must be considered in its entirety, i.e., as a **whole**, including portions that would lead away from the claimed invention. Such a teaching away from a claimed invention constitutes potent evidence of non-obviousness. See, for example, *In re Bell*, 991 F.2d 781, 26 USPQ2d 1529 (Fed. Cir. 1993); *In re Hedges*, 783 F.2d 1038, 228 USPQ 685 (Fed. Cir. 1986); *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469

U.S. 851 (1984). Tsukamoto teaches forming LDD regions that undergo high temperature anneal, which would cause dopant to diffuse out from the source/drain extensions. Hence, Tsukamoto teach away from the claimed method, and it would not be obvious to combine Tsukamoto with Bai to achieve the claimed method.

In addition, claims 8, 9, 16, and 17 are separately patentable because Tsukamoto teaches exposing the source/drain regions to laser radiation, not the source/drain extensions, as required by claims 8, 9, 16, and 17.

As regards Ozturk et al., Appellants note that the combination of Ozturk et al. and Bai does not suggest the claimed methods of manufacturing a semiconductor device because Ozturk et al. do not cure the deficiencies of Bai. Ozturk et al. do not suggest forming supersaturated dopant concentration source/drain extensions in the substrate between the source/drain regions and the gate electrode.

IX. CONCLUSION

Based upon the arguments submitted supra, Appellants respectfully submit that the Examiner's rejections under 35 U.S.C. § 103 are not legally viable. Appellants, therefore, respectfully solicit the Honorable Board to reverse the following rejections:

Claims 1-3 and 5 as obvious as evidenced by Bai and Applicant admitted prior art (AAPA);

Claim 4 as obvious as evidenced by Bai, AAPA, and Hsu;

Claims 6 and 7 as obvious as evidenced by Bai, AAPA, and Murthy et al.;

Claims 8 and 9 as obvious as evidenced by Bai, AAPA, and Tsukamoto;

Claims 10 and 11 as obvious as evidenced by Bai, AAPA, and Ozturk et al;

Claims 12 and 13 as obvious as evidenced by Bai, AAPA, and Hsu;

Claims 14 and 15 as obvious as evidenced by Bai, AAPA, Hsu, and Ozturk et al.;

Claims 16 and 17 as obvious as evidenced by Bai, AAPA, Hsu, and Tsukamoto; and

Claim 18 as obvious as evidenced by Bai, AAPA, Hsu, and Murthy et al.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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X. APPENDIX

Appealed Claims

1. A method of manufacturing a semiconductor device, the method comprising:

providing a silicon-containing substrate, having an upper surface, comprising: a gate electrode formed on the upper surface of the substrate with a gate insulating layer therebetween, the gate electrode having an upper surface and opposing side surfaces, and source/drain regions in the substrate spaced apart from the gate electrode;

forming supersaturated dopant concentration source/drain extensions in the substrate between the source/drain regions and the gate electrode; and

forming metal silicide contacts on the upper surfaces of the gate electrode and the substrate, in a manner sufficient to maintain the supersaturated dopant concentration in the source/drain extensions.

2. The method according to claim 1, wherein the temperature is maintained below about 700°C throughout the forming of the metal silicide contacts.

3. The method according to claim 2, wherein the metal silicide contacts are made of NiSi.

4. The method according to claim 3, wherein the silicon containing substrate further comprises sidewall spacers on the gate electrode opposing side surfaces, the method further comprising forming source/drain regions and subsequently removing the sidewall spacers prior to forming the source/drain extensions.

5. The method according to claim 3, wherein the step of forming the metal silicide contacts comprises:

depositing a dielectric layer over the substrate and gate electrode upper surfaces;

patterning the dielectric layer to form sidewall spacers on the gate electrode opposing side

surfaces;

depositing a nickel layer over the gate electrode upper surface, sidewall spacers, and substrate upper surface;

heating to react the nickel layer with underlying silicon in the gate electrode and source/drain regions to form the nickel silicide (NiSi) contacts;

and removing the nickel that did not react to form nickel silicide.

6. The method according to claim 3, wherein the nickel layer is heated at a temperature of about 400°C to about 600°C for about 15 seconds to about 120 seconds to form the NiSi contacts.

7. The method according to claim 3, wherein the dopant concentration in the source/drain extensions is about 10^{21} ions/cm^3.

8. The method according to claim 3, wherein the step of forming the supersaturated source/drain extensions comprises:

ion implanting a dopant; and

exposing the dopant implants to laser radiation at an energy density sufficient to anneal the dopant implants.

9. The method according to claim 8, wherein the source/drain extensions are formed at an ion implantation dosage of about $1x10^{14}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2 and an ion implantation energy of about 1 keV to about 50 keV, and with a laser radiation energy density of about 0.1 J/cm^2 to about 5.0 J/cm^2.

10. The method according to claim 3, wherein the step of forming the supersaturated source/drain extensions comprises forming the source/drain extensions by doped selective epitaxy.

11. The method according to claim 10, wherein the step of forming the source/drain extensions by doped selective epitaxy comprises:

forming an oxide layer on the semiconductor substrate and gate electrode;

patterning the oxide layer to form an oxide film on the gate opposing side surfaces;

forming an epitaxial layer by applying a gas mixture comprising SiH_4, and a dopant gas to the substrate surface at a temperature of about 700°C to about 900°C and at a pressure of about 1 torr to about 700 torr.

12. A method of manufacturing a semiconductor device, the method comprising:

providing a silicon-containing semiconductor substrate;

forming a gate oxide layer on the semiconductor substrate;

forming a conductive gate material layer over the gate oxide layer;

patterning the gate material layer and gate oxide layer to form a gate electrode having an upper surface and opposing side surfaces, with a gate oxide layer thereunder;

depositing a layer of insulating material over the gate electrode and semiconductor substrate;

patterning the insulating material to form sidewall spacers on the opposing side surfaces of the gate electrode;

forming source/drain regions by ion implanting a dopant into the substrate;

removing the sidewall spacers;

heating the substrate to activate the source/drain regions;

forming supersaturated dopant concentration source/drain extensions between the gate electrode and source/drain regions;

depositing a second layer of insulating material over the gate electrode and semiconductor substrate;

patterning the second layer of insulating material to form sidewall spacers on the opposing side surfaces of the gate electrode;

depositing a metal layer over the gate electrode upper surface, sidewall spacers, and substrate upper surface;

heating at a temperature to react the metal layer with underlying silicon to form metal silicide contacts on the gate electrode and substrate upper surfaces without reducing the dopant concentration in the source/drain extensions below a supersaturated dopant concentration; and

removing the metal that did not react to form metal silicide.

13. The method according to claim 12, wherein the metal layer is Ni.

14. The method according to claim 13, wherein the supersaturated source/drain extensions are formed by doped selective epitaxy.

15. The method according to claim 14, wherein the step of forming the source/drain extensions by doped selective epitaxy comprises;

forming an oxide layer on the gate electrode and semiconductor substrate;

patterning the oxide layer to form an oxide film on the gate electrode opposing side surfaces;

forming an epitaxial layer on the substrate by applying a gas mixture comprising SiH_4 and a dopant gas to the substrate surface at a temperature of about 700°C to about 900°C and at a pressure of about 1 torr to about 700 torr.

16. The method according to claim 13, wherein the step of forming the supersaturated source/drain extension comprises:

ion implanting a dopant; and

exposing the dopant implants to laser radiation at an energy density sufficient to anneal the

dopant implants.

17. The method according to claim 16, wherein source/drain extensions are formed at an implantation dosage of about $1x10^{14}$ ions/cm^2 to about $1x10^{16}$ cm^2 and an ion implantation energy of about 1 keV to about 50 keV, and with a laser radiation energy density of about 0.1 J/cm^2 to about 5.0 J/cm^2.

18. The method according to claim 13, wherein the dopant concentration in the source/drain extensions is about 10^{21} ions/cm^3.